REMARKS

Favorable reconsideration of the application is respectfully requested in light of the amendments and remarks herein.

Upon entry of this amendment, claims 1-42 will be pending. By this amendment, claim 24 has been canceled. Claims 1, 8, 9, 16, and 21 have been amended to address the claim objections and other informalities. No new matter has been added.

Objections to the Specification

In Section 1 of the Office Action, the Examiner has objected to the Abstract of the Disclosure. An amended Abstract is presented above in the Amendments to the Specification section. It is submitted that this amended Abstract obviates the objection and so it is respectfully requested that this objection be withdrawn.

§101 Rejection of Claim 25

In Section 4 of the Office Action, the Examiner has rejected claim 25 under 35 U.S.C. §101 for failing to define, describe or refer to any useful, concrete, and tangible feature. This rejection is respectfully traversed.

Claim 25 recites the structure of a digital signal comprising a plurality of data blocks, which is used to carry data. Each data block includes a header and at least one slot, each of which includes a slot header and a data packet. The data packet of the first slot includes a first part of the digital signal and a reference time relating to the time of production of the first part. Each data packet of the subsequent slots includes a subsequent part of the digital signal and timing information defining the time of production of the subsequent part relative to the

reference time. The structure of the digital signal, as defined above, provides greater flexibility than those of the prior art digital signals. Therefore, the digital signal as defined and described in claim 25 provides useful, concrete, and tangible features.

Based upon the foregoing, it is submitted that claim 25 does not fail to define, describe or refer to any useful, concrete, and tangible feature, as presented and referenced by the Examiner. Accordingly, it is submitted that the Examiner's rejection of claim 25 based upon 35 U.S.C. §101 has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§102 Rejection of Claims 1 and 25

In Section 6 of the Office Action, the Examiner has rejected claims 1 and 25 under 35 U.S.C. §102(e) as being anticipated by Fujii *et al.* (U.S. Patent 5,966,385; hereinafter referred to as "Fujii"). This rejection is respectfully traversed below.

Claims 1 and 25 teach a digital signal and an encoder for encoding the digital signal. The digital signal comprises a plurality of data blocks, which is used to carry data. Each data block includes a header and at least one slot, each of which includes a slot header and a data packet. The data packet of the first slot includes a first part of the digital signal and a reference time relating to the time of production of the first part. Each data packet of the subsequent slots includes a subsequent part of the digital signal and timing information defining the time of production of the subsequent part relative to the reference time.

It was described in the Background section of the Specification that transmission of the packetized signals, such as MPEG 2 Transport Stream (TS), over interfaces, such as Serial Data Transport Interface (SDTI), "requires buffering to ensure that the packets are confined to the payload area of the SDTI and to allow multiple packets on each line for efficiency." *Page 1,*

lines 22-24 of the Specification. However, the "buffering process introduces delay and jitter (i.e., variation in the timing of the packets relative to each other) to the packets but, for accurate decoding of an MPEG 2 signal, the packets of that signal must be provided to the MPEG decoder with accurate timing relative to one another to allow correct decoding. Whilst absolute delay of packets is not a problem because it affects all packets equally, there is a need to correct jitter at or before the MPEG decoder." *Page 1, lines 24-30 of the Specification.*

The structure of the digital signal described in claims 1 and 25 is designed to overcome the above-described shortcomings of the prior packetized signal structure. Specifically, the timing information available for every packet relative to the reference time (*i.e.*, the time of production of the first packet) substantially reduces the timing jitter introduced by the buffering of data in preparation for transmission of data over interfaces such as SDTI. Thus, the structure of the digital signal, as defined above, provides greater flexibility than those of the prior art digital signals.

It appears that Fujii discloses a transmission system configured to decode TS packets, which may contain a time reference referred to as a program clock reference (PCR). The PCR is used to synchronize the video data with the audio data. Fujii however fails to teach or suggest maintaining relative timing information between each packet slot and the time reference that would indicate the relative time of production of data blocks or chunks as stored in a transmission buffer so that those blocks or chunks can be reconstituted with minimal jitter in the data.

Based upon the foregoing, it is submitted that claims 1 and 25 are not anticipated by the teachings of Fujii, as presented and referenced by the Examiner. Accordingly, it is submitted

that the Examiner's rejection of claims 1 and 25 based upon 35 U.S.C. §102(e) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§102 Rejection of Claim 24

In Section 7 of the Office Action, the Examiner has rejected claim 24 under 35 U.S.C. §102(e) as being anticipated by Hurst *et al.* (U.S. Patent 6,141,358; hereinafter referred to as "Hurst"). This rejection is obviated by the cancellation of claim 24.

§103 Rejection of Claims 2-8 and 26-33

In Section 9 of the Office Action, the Examiner has rejected claims 2-8 and 26-33 under 35 U.S.C. §103(a) as being unpatentable over Fujii, as applied to claims 1 and 25 above, and in view of O'Grady (U.S. Patent 6,195,392). This rejection is respectfully traversed below.

As discussed above, the structure of the digital signal described in claims 1 and 25 is designed to overcome the shortcomings of the prior packetized signal structure. Specifically, the timing information available for every packet relative to the reference time (*i.e.*, the time of production of the first packet) substantially reduces the timing jitter introduced by the buffering of data in preparation for transmission of data over interfaces such as SDTI. Thus, the structure of the digital signal provides greater flexibility than those of the prior art digital signals.

Claims 2-8 and 26-33 depend from claims 1 and 25, respectively. Therefore, claims 2-8 and 26-33 should be allowable over Fujii. Further, the Examiner indicates in Section 9 of the Office Action that "O'Grady discloses an apparatus that eliminates the need for these expensive components presently necessary in the state of the art PCR generators (O'Grady: column 1, line 66 to column 2, line 9)." It appears that O'Grady teaches an apparatus for enhancing the current

reference time generator, but fails to teach or suggest providing timing information of parts of the digital signal relative to the reference time. Therefore, it does not appear that the arguments presented by the Examiner in rejecting claims 2-8 and 26-33 establish how the combination of Fujii and O'Grady teaches or suggests the digital signal with a structure that is designed to overcome the shortcomings of the prior packetized signal structure.

Based upon the foregoing, it is submitted that claims 2-8 and 26-33 are not rendered obvious by the teachings of Fujii and O'Grady, as presented and referenced by the Examiner. Accordingly, it is submitted that the Examiner's rejection of claims 2-8 and 26-33 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§103 Rejection of Claims 16-23 and 34

In Section 10 of the Office Action, the Examiner has rejected claims 16-23 and 34 under 35 U.S.C. §103(a) as being unpatentable over Fujii, as applied to claims 1 and 25 above, and in view of O'Grady and Lenihan *et al.* (U.S. Patent 6,169,843; hereinafter referred to as "Lenihan"). This rejection is respectfully traversed below.

As discussed above with respect to claims 1 and 25, and claims 2-8 and 26-33, claims 16-23 teach a decoder for decoding the same digital signal recited in claims 1 and 25. Claim 34 depends from claim 25. Therefore, claims 16-23 and 34 should be allowable over Fujii and O'Grady because these references are not suggestive of the signals that these claims recite. Further, it appears Lenihan teaches a decoder that can remove or ignore any null packets in incoming transport streams such that only valid packets are made available, but fails to teach or suggest providing timing information of parts of the digital signal relative to the reference time.

Therefore, it does not appear that the arguments presented by the Examiner in rejecting claims 16-23 and 34 establish how the combination of Fujii, O'Grady, and Lenihan teaches or suggests the digital signal with a structure that is designed to overcome the shortcomings of the prior packetized signal structure.

Based upon the foregoing, it is submitted that claims 16-23 and 34 are not rendered obvious by the teachings of Fujii, O'Grady, and Lenihan, as presented and referenced by the Examiner. Accordingly, it is submitted that the Examiner's rejection of claims 16-23 and 34 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

§103 Rejection of Claims 9-15 and 35-42

In Section 11 of the Office Action, the Examiner has rejected claims 9-15 and 35-42 under 35 U.S.C. §103(a) as being unpatentable over Fujii, as applied to claims 1 and 25 above, and in view of Hurst. This rejection is respectfully traversed below.

As discussed above, the structure of the digital signal described in claims 1 and 25 is designed to overcome the shortcomings of the prior packetized signal structure. Specifically, the timing information available for every packet relative to the reference time (*i.e.*, the time of production of the first packet) substantially reduces the timing jitter introduced by the buffering of data in preparation for transmission of data over interfaces such as SDTI. Thus, the structure of the digital signal provides greater flexibility than those of the prior art digital signals.

Claims 9-15 and 35-42 depend from claims 1 and 25, respectively. Therefore, claims 9-15 and 35-42 should be allowable over Fujii. Further, the Examiner indicates in Section 11 of the Office Action that "Hurst teaches that blocks of data do not need to be evenly distributed or

of similar size in order to be transported within an SDTI system (Hurst: column 3, lines 62-64, wherein the chunks are the blocks of data)." Thus, it appears that Hurst teaches variable length data blocks, but fails to teach or suggest providing timing information of parts of the digital signal relative to the reference time. Therefore, it does not appear that the arguments presented by the Examiner in rejecting claims 9-15 and 35-42 establish how the combination of Fujii and Hurst teaches or suggests the digital signal with a structure that is designed to overcome the shortcomings of the prior packetized signal structure.

Based upon the foregoing, it is submitted that claims 9-15 and 35-42 are not rendered obvious by the teachings of Fujii and Hurst, as presented and referenced by the Examiner. Accordingly, it is submitted that the Examiner's rejection of claims 9-15 and 35-42 based upon 35 U.S.C. §103(a) has been overcome by the present remarks and withdrawal thereof is respectfully requested.

Conclusion

In view of the foregoing, entry of this amendment, and the allowance of this application with claims 1-23 and 25-42 are respectfully solicited.

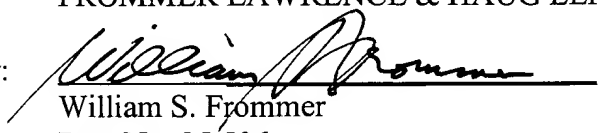
In regard to the claims amended herein and throughout the prosecution of this application, it is submitted that these claims, as originally presented, are patentably distinct over the prior art of record, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes to these claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these changes are made simply for clarification and to round out the scope of protection to which Applicant is entitled.

In the event that additional cooperation in this case may be helpful to complete its prosecution, the Examiner is cordially invited to contact Applicant's representative at the telephone number written below.

The Commissioner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP

By: 

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